MOSTEK®

Z80 MICROCOMPUTER SYSTEMS

Operations Manual

FLP-80 DOS/MDX DISK OPERATING SYSTEM V2.1

FLP-80DOS/MDX

DISK OPERATING SYSTEM

VERSION 2.1

MK77962

MOSTEK reserves the right to make changes in specifications at any time and without notice. The information furnished by MOSTEK in this publication is believed to be accurate and reliable; however, no responsibility is assumed by MOSTEK for its use, nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of MOSTEK.

Publication Number MK79668

TABLE OF CONTENTS

SECTION NUMBER	PARAGRAPH NUMBER	TITLE	PAGE NUMBER
1		OVERVIEW AND OPERATION	
	1-1	INTRODUCTION	1-1
	1-4	REFERENCES	1-1
	1-5	CONVENTIONS USED IN THIS MANUAL	1-1
	1-7	HARDWARE CONFIGURATION	1-2
	1-10	MDX-EPROM/UART JUMPER OPTIONS	1-2
	1-13	MDX-DRAM JUMPER OPTIONS	1-3
	1-17	MDX-CPU1 JUMPER OPTIONS	1-3
	1-19	MDX-FLP JUMPER OPTIONS	1-4
	1-21	POWER REQUIREMENTS	1-4
	1-24	CONNECTING THE RESET SWITCH	1-5
	1-26	FLEXIBLE DISK DRIVE OPTIONS	1-5
	1-28	SYSTEM CONNECTION	1-5
	1-32	INITIAL POWER-UP	1-6
2		DIFFERENCES IN THE FLP-80DOS AND FLP-80DOS/MDX SYSTEMS	
	2-1	INTRODUCTION	2-1
	2-3	HARDWARE DIFFERENCES	2-1
	2-6	SOFTWARE DIFFERENCES	2-1
APPENDIX A		PPG-8/16 PROM PROGRAMMER CONNECTION	A-1
APPENDIX B		CENTRONICS LINE PRINTER CONFIGURATION	B-1

LIST OF TABLES

TABLE NUMBER	DESCRIPTION	PAGE NUMBER
1-1	MDX-EPROM/UART BAUD RATE SELECTION TABLE	1-7
1-2	SHUGART SA800 AC REQUIREMENTS	1-8
1-3	SHUGART SA800 DC REQUIREMENTS (EACH DRIVE)	1-9
1-4	WIRE LIST FOR MDX-FLP J2 CONNECTOR	1-10
1-5	WIRE LIST FOR UART TO TTY CABLE	1-11
2-1	PORT ASSIGNMENT SUMMARY	2-3

SECTION 1

OVERVIEW AND OPERATION

1-1. INTRODUCTION

1-2. FLP-80DOS/MDX is a complete floppy disk operating system for the Mostek MDX board series. It is identical in function to the Mostek FLP-80DOS Operating System used on Mostek Development Systems. The package consists of two 2716 PROM's and a standard FLP-80DOS diskette configured for 32K of RAM.

1-3. The intent of this manual is to act as a supplement to the FLP-80DOS Operations Manual, MK78557, for users with a MDX-FLP system. The FLP-80DOS manual is correct for all MDX-FLP functions except for those differences outlined in this manual. Board requirements, hardware options, initial power-up procedures, and differences between the FLP-80DOS and MDX-FLP systems are covered in the following sections.

1-4. REFERENCES

AID-80F Operations Manual, MK78569
SYS-80F Operations Manual, MK78576
FLP-80DOS Operations Manual, MK78557
MDX-DRAM Operations Manual, MK79624
MDX-EPROM/UART Operations Manual, MK79604
MDX-FLP Operations Manual, MK79639
MDX-CPU1 Operations Manual, MK79612

1-5. CONVENTIONS USED IN THIS MANUAL

1-6. All user input is underlined. Those items which must be entered exactly as shown are upper case. Those items which are variable are lower case. The symbol <CR> stands for carriage return.

1-7. HARDWARE CONFIGURATION

1-8. This section outlines procedures for configuring a 32K byte FLP-80DOS/MDX system with a 2.5 MHZ system clock. It is assumed that the user will supply all power required for the disk drives and the card cage. The following hardware is required as a minimum to construct a 32K byte flexible disk system:

MDX-EPROM/UART	MK77753
MDX-CPU1	MK77850
MDX-DRAM 32	MK77752
MDX-FLP	MK77652
MD-CC8 Card Cage	MK77954
MD-TTY Cable	MK77956
Disk Drive Cable	See Table 1-4.
Disk Drives (8",2)	See MDX-FLP Ops Man for vendors/models

1-9. Each board has some jumper options to allow different addressing and hardware configurations. The following sections discuss the options for configuring a standard 32K flexible disk system using the above mentioned boards.

1-10. MDX-EPROM/UART JUMPER OPTIONS

1-11. The MDX-EPROM/UART provides the system designer with sockets to contain up to 10K x 8 of ROM or EPROM memory. This storage area is not required for operation with the FLP-80DOS/MDX system. Jumpers in socket J2 and pins E1 through E8 are related to the addressing and selection of the ROM/EPROM sockets. The user should refer to the MDX-EPROM/UART Operations Manual (MK79604) for instructions if ROMS or EPROMS are desired here.

1-12. The system Baud Rate Generator is also contained on the EPROM/UART board and must be set up to match the baud rate of the console device. Table 1-1 shows the configuration of switch pack U8 for various baud rates.

1-13. MDX-DRAM JUMPER OPTIONS

1-14. The MDX-DRAM board is available in three memory capacities. The scope of this manual is to provide set-up instructions for a 32K system only. Additional information for other configurations is available in the MDX-DRAM Operations Manual (MK79624).

1-15. Jumpers on the MDX-DRAM board control the memory configuration. A 32K RAM board should be populated with 16 MK4116 RAMs and have the following jumpers installed on the board:

B to C
E to F
H to J

1-16. Switch pack U28 controls the starting address for the memory board. For a typical 32K RAM system, memory should begin at location 0000H. To select location 0000H, position all four switches on U28 to the "open" position.

1-17. MDX-CPU1 JUMPER OPTIONS

1-18. The MDX-CPU1 board should have two 2716 EPROMs containing DDT and the Disk Controller Firmware (DCF) origined at E000H. These EPROMs are supplied as part of the FLP-80DOS/MDX software package. Jumper options on the board control the Reset address, EPROM start addresses, wait states, and the 256 x 8 static RAM enable circuitry. Jumpers on sockets U5 and U10 should be configured for operation as a FLP-80DOS/MDX system as follows:

U5 pin 2 to pin 3
pin 4 to pin 14
pin 5 to pin 13

U10 pin 2 to pin 3
pin 6 to pin 8
pin 9 to pin 10

All other pins on U5 and U10 should be open.

1-19. MDX-FLP JUMPER OPTIONS

1-20. The MDX-FLP board offers jumpers to control the port addressing and some control functions. For correct operation with the FLP-80DOS/MDX package, the user should install the following jumpers. Any other jumpers should be removed from the board.

E2	Select 8" Drives
E5	" " "
E7	" " "
E8	" " "
E12	Select Port Address E0H
E13	" " " "
E4	Select Single-Sided Drives (remove for double-sided)

1-21. POWER REQUIREMENTS

1-22. Power should be connected to the MD-CC8 card cage by attaching power supply lines to a mating connector (Viking 3VH28/1CND5 or equivalent) as follows:

Connector Pin	Voltage	Max Current Rating
1,2	+5V	4.1A
3,4	GND	-
55	+12V	0.3A
56	-12V	0.08A

1-23. Power should be connected to a Shugart SA800 disk drive as described in Tables 1-2 and 1-3. For other drive types, the user should consult the Operations Manual for the type of drive selected for power connections.

1-24. CONNECTING THE RESET SWITCH

1-25. A "system reset" switch should be added by the user by connecting a "momentary - normally open" switch between pin 3 (GND) and pin 48 (PBRESET) of the card cage connector.

1-26. FLEXIBLE DISK DRIVE OPTIONS

1-27. Disk drives should be configured with the correct options for use with the MDX-FLP hardware and system software. The following list describes the jumpers required for Shugart SA800 or SA850 drives. For other types of disk drives, consult the Disk Drive User's Guide for assistance.

1. All Drives - Y,A,B,800,DS,C,T2,L
2. Last Drive - T1,T3,T4,T5,T6
   of daisy chain
3. Drive Select - Drive 0 - DS1
   Drive 1 - DS2
   Drive 2 - DS3
   Drive 3 - DS4

1-28. SYSTEM CONNECTION

1-29. After power connections have been made to the disk drives and to the card cage, the user should check for correct voltages on the connector pins before attempting to insert any cards into the rack. Power should always remain off while inserting or removing cards.

1-30. At this point, the user may insert all of the MD Series cards into the card cage and connect the TTY cable to the J1 connector of the MDX-EPROM/UART board and the console device. The MDX-FLP card must be inserted as the highest priority card (left most card for the Mostek card cage) among cards having interrupt capability (FLP and CPU1 in minimum configuration as described earlier). There should be no empty card slots (breaks in the PCO/PCI chain) between the FLP card and the last (right most) card having interrupt capability.

1-31. The disk drive cable may be connected to the J2 connector of the MDX-FLP card and the disk drives being used. Table 1-4 shows a wiring list for Shugart SA800 drives and table 1-5 shows a wiring list for the UART connector. The user should consult the Operations Manual of the disk drive being used if other than a Shugart SA800 or SA850.

1-32. **INITIAL POWER-UP**

1-33. After all the above steps have been performed and checked, the user may turn on power to the system and start operation. After power has been applied, the MOSTEK system disk shipped with the FLP-80DOS/MDX package may be inserted in disk unit 0 and the disk drive door closed. The user should then press the "reset" switch and the Return key on the console device. The system should respond by loading the Operating System from disk unit 0 and print the following message to the console device:

```
MOSTEK FLP-80DOS Vn.n   (n.n should be 2.1 or later)
$
```

If the user does not get the correct response, the following items should be done:

1. Check the power supply levels on the MD-CC8 connector.
2. Check the jumper options on each MD card.
3. Ensure that each card is seated properly in the connectors.
4. Check the jumper options on each disk drive.
5. Check the cables to the console device and disk drives.
6. Check to see that the disk is in disk unit 0 and that it is the Mostek system disk.
7. Make sure that the baud rate of the console device matches the baud rate selected on the MDX-EPROM/UART board.

1-34. If the above procedures fail to give the correct response, check with your local FAE or call MOSTEK for assistance.

TABLE 1-1
MDX-EPROM/UART BAUD RATE SELECTION TABLE

U8 Switch Options

POSITION 4	3	2	1	X16 CLOCK	BAUD RATE
0	0	0	0	.8KHZ	50
0	0	0	1	1.2	75
0	0	1	0	1.76	110
0	0	1	1	2.1523	134.5
0	1	0	0	2.4	150
0	1	0	1	4.8	300
0	1	1	0	9.6	600
0	1	1	1	19.2	1200
1	0	0	0	28.8	1800
1	0	0	1	32.081	2000
1	0	1	0	38.4	2400
1	0	1	1	57.6	3600
1	1	0	0	76.8	4800
1	1	0	1	115.2	7200
1	1	1	0	153.6	9600
1	1	1	1	316.8	19200

1 = OPEN 0 = CLOSED

TABLE 1-2

SHUGART SA800 AC REQUIREMENTS

SHUGART P4 PIN	60 HZ		50 HZ	
	115 V (STANDARD)	208/230 V	110 V	220 V
1 2 3	85-127 VAC FRAME GND 85-127 VRTN	170-253 VAC FRAME GND 170-253 VTRN	85-127 VAC FRAME GND 85-127 VRTN	170-253 VAC FRAME GND 170-253 VRTN
MAX CURRENT	0.5 AMPS	0.4 AMPS	0.6 AMPS	0.4 AMPS
FREQ TOLERANCE	+- 0.5 HZ			

TABLE 1-3
SHUGART SA800 DC REQUIREMENTS (EACH DRIVE)

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (P TO P)
1	+24 VDC	±1.2VDC	1.7 A MAX 1.3 A TYP	100 mV
2	+24 V RETURN			
3	- 5 V RETURN			
4	- 5 VDC	±0.25 VDC	0.07 A MAX 0.05 A TYP	50 mV
	Optional - 7 to - 16VDC (Cut Trace 'L')	NA	0.10 A MAX 0.07 A TYP	NA
5	+ 5 VDC	±0.25 VDC	1.0 A MAX 0.8 A TYP	50 mV
6	+ 5 V RETURN			

1-35. NOTE: Assure that the proper model has been selected to correspond to input voltage requirements. Power for the flexible disk drives is shown for a single Shugart SA800 drive. Refer to the SA800 or SA850 DISKETTE STORAGE DRIVE OEM manual for more details.

TABLE 1-4

WIRE LIST FOR MDX-FLP J2 CONNECTOR

Pin	Description
14	/SS (8")
16	/SS (5")
18	/HLD
20	/INDEX (8")
22	/RDY
24	/INDEX (5")
26	/DS1
28	/DS2
30	/DS3
32	/DS4
34	/DIRC
36	/STEP
38	/WD
40	/WG
42	/TRACK 0
44	/WTPT
46	/RDDATA

All odd pins ground

TABLE 1-5

WIRE LIST FOR UART TO TTY CABLE

PIN	DESCRIPTION
1	Chassis GND
2	Transmitted Data
3	Received Data
16	Reader Step +
4	Request to Send
5	Clear to Send
6	Data Set Ready
7	GND
20	Data Terminal Ready
8	Carrier Detect
21	Reader Step -
24	20 mA+ Receive (RX+)
12	20 mA- Receive RET (RX-)
25	20 mA- Send (TX-)
13	20 mA+ Send (TX+)

SECTION 2

DIFFERENCES IN THE FLP-80DOS AND FLP-80DOS/MDX SYSTEMS

2-1. INTRODUCTION

2-2. The MDX-FLP board requires that the Disk Controller Firmware (DCF) be different from that of the FLP-80DOS firmware due to the use of the DMA chip on the MDX-FLP board. Most of the changes are transparent to the user who has developed software under FLP-80DOS, but a few could have an effect on user operation. These changes are listed in the following paragraphs. FLP-80DOS users should read this section carefully and be aware of all the differences.

2-3. HARDWARE DIFFERENCES

2-4. The Counter Timer Circuit chip (CTC) on the MDX-CPU1 board uses ports 7C and 7D. FLP-80DOS uses ports D8 and D9 for the CTC. To allow software interchangability between FLP-80DOS/MDX and FLP-80DOS, both sets of ports are handled by FLP-80DOS software, release 2.1 and later. Therefore, the user should make sure that these ports are not used or modified by any user program, or used for any additional boards in the system.

2-5. Table 2-1 lists the ports used by the system and the function of each port. The user should exercise caution when using these ports to avoid conflict with the Operating System.

2-6. SOFTWARE DIFFERENCES

2-7. Registers A and F of the Z80 register map (OFFFCH and OFFFDH) in DDT are modified when a System Reboot occurs, if disk unit 0 is ready. This should not affect the user since the registers are not normally of interest after a System Reboot.

2-8. The FLP-80DOS system measures and sets the baud rate to match the console device on boot-up. The MD system measures the baud rate but does not set it. This is performed by switch options on the MDX-EPROM/UART board (see section 1-11).

2-9. Section 11 of the FLP-80DOS Operations Manual describes the calling conventions of the Disk Controller Firmware. This information is correct except that I/O is performed by a DMA chip rather than by a hardware FIFO. Also, the Interactive Save command (E006H) is no longer available.

TABLE 2-1

PORT ASSIGNMENT SUMMARY

PORT ADDRESSES

PORT (HEX)	READ	WRITE
7C	CTC Channel 0	CTC Channel 0
7D	CTC Channel 1	CTC Channel 1
D8	CTC Ch 0 (SDB series)	CTC Ch 0 (SDB series)
D9	CTC Ch 1 (SDB series)	CTC Ch 1 (SDB series)
DC	UART Data	UART Data
DD	UART Control	UART Control
DE	Serial Control	Serial Control
E0	DMA Controller	DMA Controller
E1	Undefined	Undefined
E2	Status to CPU	
E3	Control to CPU	Control from CPU
E4	Status Register	Command Register
E5	Track Register	Track Register
E6	Sector Register	Sector Register
E7	Data Register	Data Register

INPUT PORT E2H

BIT

0 Double sided
1 Interrupt
2 NU
3 NU
4 NU
5 8" Floppy
6 NU
7 NU

NU = not used

INPUT/OUTPUT PORT E3H

BIT

0 Drive 1 selected
1 Drive 2 secected
2 Drive 3 selected
3 Drive 4 selected
4 Side two select
5 NU
6 NU
7 NU

INPUT PORT E4H	STATUS REGISTER
OUTPUT PORT E4H	COMMAND REGISTER
I/O PORT E5H	TRACK REGISTER
I/O PORT E6H	SECTOR REGISTER
I/O PORT E7H	DATA REGISTER

(See MDX-FLP Operations Manual for information on these ports)

APPENDIX A

PPG-8/16 PROM PROGRAMMER CONNECTION

PPG-8/16 PROM PROGRAMMER CONNECTION

A-1. The PPG-8/16 PROM PROGRAMMER may be connected to the MDX-FLP System by using a MDX-PIO board (MK77650) with the following jumper options and cable. The power cable for the PPG-8/16 may be created by using information contained in the PPG-8/16 Operations Manual (MK79603) or purchased from Mostek (PN MK77957).

A-2. Uses Ports D4H,D5H,D6H,D7H on Connector J2 of MDX-PIO

A-3. NOTE: The PPG-08 PROM PROGRAMMER is connected in the same manner as the PPG-8/16 except a different cable is required for connection to the PPG-08 J1 connector (See PPG-08 Operations Manual (MK78532) for signal description).

Install jumpers as follows:	Remove jumpers as follows:
J3-E6	J3-E14
J3-E8	J3-E16
J3-E10	J3-E20
J3-E11	J3-E24
J3-E18	J4-E1
J3-E22	J4-E2
J4-E3	J4-E4
J4-E5	

Remove resistor packs UR3 and UR4.

WIRING LIST FOR PPG-8/16 TO MDX-PIO

MDX-PIO J2 CONNECTOR	PPG-8/16 J3 CONNECTOR
2	10
19	1
6	2
18	3
5	4
17	5
4	6
16	7
3	8
7	20
20	21
8	11
21	12
9	13
22	14
10	15
23	16
11	17
25	23
24	24

APPENDIX B

CENTRONICS LINE PRINTER CONFIGURATION

CENTRONICS 702 LINE PRINTER CONNECTION

B-1. The Centronics Model 702 Line Printer may be connected to the MDX-FLP System by using the MDX-PIO board (MK77650) with the following jumper options and cable.

B-2. Uses Ports D0H,D1H,D2H,D3H on connector J1 of MDX-PIO

Install jumpers as follows:	Remove jumpers as follows:
J3-E7	J3-E9
J3-E15	J3-E17
J4-E3	J3-E19
J4-E5	J3-E21
	J3-E23
	J3-E25
	J4-E1
	J4-E2
	J4-E4

Install IC 74LS242 in socket U2 (shipped as 74LS243).

WIRING LIST FOR CENTRONICS 702 PRINTER TO MDX-PIO

MDX-PIO J1 CONNECTOR	CENTRONICS CONNECTOR
19	6
6	8
18	10
5	12
17	14
4	16
16	18
3	20
7	26
9	34
22	36
11	24
24	5
25	7
14	9
15	11

MOSTEK®
Z80·F8 Covering the full spectrum of
3870 microcomputer applications.

1215 W. Crosby Rd. • Carrollton, Texas 75006 • 214/323-6000
In Europe, Contact: MOSTEK Brussels
150 Chaussee de la Hulpe, B1170, Belgium;
Telephone: 660.69.24

Mostek reserves the right to make changes in specifications at any time and without notice. The information furnished by Mostek in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Mostek for its use; nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Mostek.

PRINTED IN USA May 1979
Publication No. MK79668

Copyright 1979 by Mostek Corporation
All rights reserved